

WHAT IS CLAIMED IS:

PATENT CLAIMS

1. Data storage device that, in response to a data output request, outputs stored data beginning with a selected output start address, characterized in that the selectable output start addresses exhibit such slight spacings from one another that the amount of data that can be stored between neighboring output start addresses is smaller than the amount of data output in response to a data output request.

2. Data storage device according to claim 1, characterized in that the determination of the output start address to be employed ensues taking address data applied to the data storage device into consideration.

3. Data storage device according to claim 2, characterized in that the determination of the output start address to be employed ensues given additional consideration of adaptation data applied to the data storage device, whereby the adaptation data defined whether and, as warranted, to what extent the output start address to be employed is higher or lower than the address that is defined by the address data.

4. Data storage device according to claim 3, characterized in that the adaptation data are employed for controlling an interface provided between the memory cells of the data storage device and the output terminals of the data storage device.

5. Data storage device according to claim 4, characterized in that the interface contains a multiplexer (MUX) that is driven by the adaptation data or based on the adaptation data, and with which the data stored beginning with a first output start address or the data stored beginning with a second output start address are optionally through-connected.

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See amended  
claims  
Substantive  
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6. Data storage device according to claim 5, characterized in that the first output start address is the address that is represented by the address data applied to the data storage device.

5 7. Data storage device according to claim 5 or 6, characterized in that the second output start address is greater or smaller than the first output start address by a scope defined by the wiring of the multiplexer (MUX).

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